WHAT IS CLAIMED IS:

1. A method of forming a semiconductor non-volatile memory cell, comprising:

forming a first insulating layer over a substrate region;

forming a first doped polysilicon layer over the first insulating layer;

forming a first undoped polysilicon layer over and in contact with the first doped polysilicon layer, the first doped and first undoped polysilicon layers forming a floating gate;

forming a second insulating layer over and in contact with the first undoped polysilicon layer;

forming a second updoped polysilicon layer over and in contact with the second insulating layer; and

forming a second doped polysilicon layer over and in contact with the second undoped polysilicon layer, the second doped and undoped polysilicon layers forming a control gate.

2. The method of claim 1 further comprising:

before said first doped polysilicon forming act, forming a third undoped polysilicon layer over and in contact with the first insulating layer wherein the first doped polysilicon layer overlies and is in contact with the third undoped polysilicon layer, the third undoped polysilicon layer forming part of the floating gate.

3. The method of claim 1 wherein the first insulating layer is a tunnel oxide layer and the second insulting layer is one of composite oxide-nitride-oxide dielectric layer and composite oxide-nitride-oxide-nitride dielectric layer .

4. The method of claim 1 wherein a thickness of each doped polysilicon layer is greater than a thickness of a corresponding undoped polysilicon layer by a factor in the range of two to four.

5. The method of claim 1 further comprising:

forming insulating spacers along sidewalls of the stack made up of the first insulting layer, the floating gate, the second insulating layer, and the control gate; and

forming source and drain regions in the substrate.

6. (Amended) The method of claim 1 wherein each of said first and second doped polysilicon layers forming acts comprises depositing an in-situ doped polysilicon layer.

7. The method of claim 1 wherein the memory cell is any one of a stacked-gate non-volatile cell and a split gate non-volatile cell.

8. The method of claim 1 wherein each of the first and second doped polysilicon layers has a doping concentration and a thickness greater than a thickness of the corresponding first and second undoped polysilicon layers so as to prevent polysilicon depletion in each of the floating gate and the control gate.

9. The method of claim 1 wherein the non-volatile memory cell is any one of ROM, flash EPROM, and EEPROM.

10. A method of forming a semiconductor transistor, comprising:

forming an insulating layer over a substrate region;

forming an undoped polysilicon layer over and in contact with the insulating layer; and

forming a doped polysilicon layer over and in contact with the undoped polysilicon layer, the doped and undoped polysilicon layers forming a gate of the transistor.

11. The method of claim 10 wherein the insulating layer is a gate oxide layer.

12. The method of claim 10 wherein a thickness of the doped polysilicon layer is greater than a thickness of the undoped polysilicon layer by a factor in the range of two to four.

13. The method of claim 10 further comprising:

forming insulating spacers along sidewalls of the gate; and

forming source and drain regions in the substrate.

14. (Amended) The method of claim 10 wherein said doped polysilicon layer forming act comprises depositing an in-situ doped polysilicon layer.

15. The method of claim 10 wherein the transistor is any one of a NMOS transistor, PMOS transistor, enhancement transistor, and depletion transistor.

16. The method of claim 10 wherein the doped polysilicon layer has a doping concentration and a thickness greater than a thickness of the undoped polysilicon layer so as to prevent polysilicon depletion in the gate.

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17. A semiconductor non-volatile memory cell comprising:

a first insulating layer over a substrate region;

a first doped polysilicon layer over the first insulating layer;

a first undoped polysilicon layer over and in contact with the first doped polysilicon layer, the first doped and first undoped polysilicon layers forming a floating gate;

a second insulating layer over and in contact with the first undoped polysilicon layer;

a second updoped polysilicon layer over and in contact with the second insulating layer; and

a second doped polysilicon layer over and in contact with the second undoped polysilicon layer, the second doped and undoped polysilicon layers forming a control gate.

SUB B1

18. The memory cell of claim 17 further comprising a third undoped polysilicon layer over and in contact with the first insulating layer wherein the first doped polysilicon layer overlies and is in contact with the third undoped polysilicon layer, the third undoped polysilicon layer forming part of the floating gate.

19. The memory cell of claim 17 wherein the first insulating layer is a tunnel oxide layer and the second insulting layer is one of a composite oxide-nitride-oxide dielectric layer and a composite oxide-nitride-oxide-nitride dielectric layer.

20. The memory cell of claim 17 wherein a thickness of each doped polysilicon layer is greater than a thickness of a corresponding undoped polysilicon layer by a factor in the range of two to four.

21. The memory cell of claim 17 further comprising:

insulating spacers along sidewalls of the stack made up of the first insulting layer, the floating gate, the second insulating layer, and the control gate; and

source and drain regions in the substrate.

SUB A2

22. The memory cell of claim 17 wherein each of said first and second doped polysilicon layers comprises are in-situ doped with impurities.

23. The memory cell of claim 17 wherein the memory cell is any one of a stacked-gate cell and split gate cell.

24. The memory cell of claim 17 wherein each of the first and second doped polysilicon layers has a doping concentration and a thickness greater than a thickness of the corresponding first and second undoped polysilicon layers so as to prevent polysilicon depletion in each of the floating gate and the control gate.

25. The memory cell of claim 17 wherein the non-volatile memory cell is any one of ROM, flash EPROM, and EEPROM.

26. A semiconductor transistor comprising:
an insulating layer over a substrate region;
an undoped polysilicon layer over and in contact with the insulating layer; and
a doped polysilicon layer over and in contact with the undoped polysilicon layer, the doped and undoped polysilicon layers forming a gate of the transistor.

27. The transistor of claim 26 wherein the insulating layer is a gate oxide layer.

28. The transistor of claim 26 wherein a thickness of the doped polysilicon layer is greater than a thickness of the undoped polysilicon layer by a factor in the range of two to four.

29. The transistor of claim 26 further comprising:
insulating spacers along sidewalls of the gate; and
source and drain regions in the substrate.

30. The transistor of claim 26 wherein the doped polysilicon layer is in-situ doped with impurities.

31. The transistor of claim 26 wherein the transistor is any one of a NMOS transistor, PMOS transistor, enhancement MOS transistor, and depletion MOS transistor.

32. The transistor of claim 26 wherein the doped polysilicon layer has a doping concentration and a thickness greater than a thickness of the undoped polysilicon layer so as to prevent polysilicon depletion in the gate.

Sub A4

33. A semiconductor structure comprising:

an undoped polysilicon layer;

a doped polysilicon layer in contact with the undoped polysilicon layer; and

an insulating layer in contact with the undoped polysilicon layer, wherein the undoped polysilicon layer is sandwiched between the doped polysilicon layer and the insulating layer.

34. The structure of claim 33 wherein a thickness of the doped polysilicon layer is greater than a thickness of the undoped polysilicon layer by a factor in the range of two to four.

35. The structure of claim 33 wherein the structure is one of a ROM cell, a flash EPROM cell, an EEPROM cell, a DRAM cell, and a SRAM cell, a NMOS transistor, a PMOS transistor, an enhancement MOS transistor, and a depletion MOS transistor.